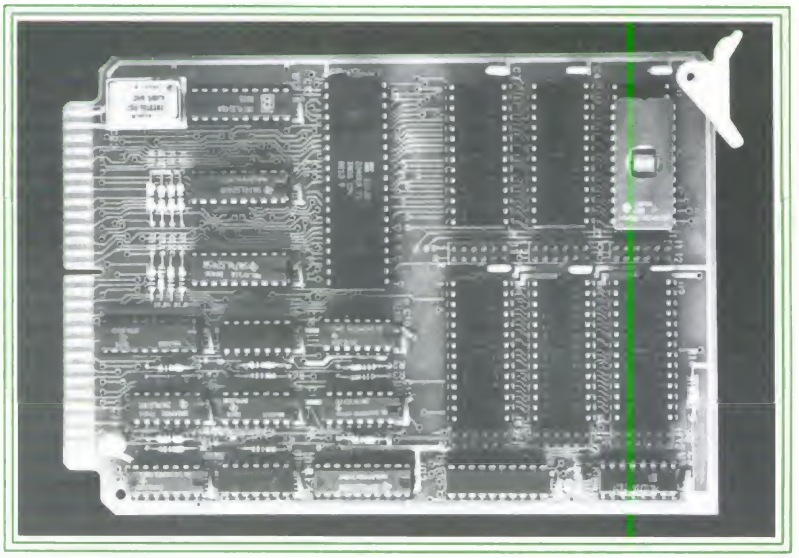
COLEX™

STD-CPUE

STD BUS



FEATURES

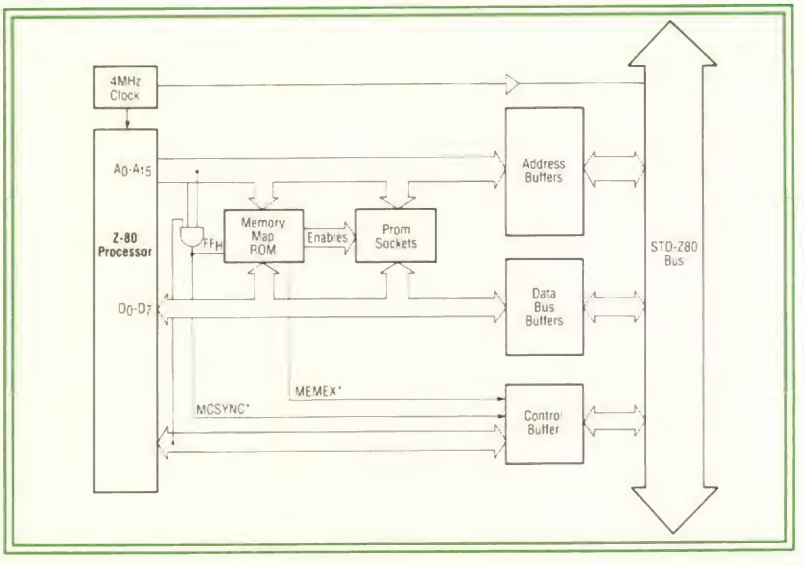
- Z80 Microprocessor
- All Signals Fully Bus Buffered
- STD-Z80 Bus Compatible
- Six 28 Pin sockets for Industry Standard ROM's, EPROM's or RAM's
- Flexible Memory Decoding on any 2K Boundary
- Phantom PROM Capability
- DMA to Onboard Memory Capability
- Supports Memory Bank Switching
- Automatic, Transparant Dynamic Memory Refresh
- 4.0 MHz operation
- 1 Year Warranty
- Single +5 Volt Supply

DESCRIPTION

The STD-CPUE is designed to be an extremely cost effective Z80 based STD Bus CPU with six 28-pin memory sockets for RAM, ROM or EPROM. An on-board memory configuration PROM supports a very flexible memory map configuration. This PROM allows up to 8 different map configurations. Each map is selectable under software control. Additionally, the user may reprogram the PROM to select his own special configurations. The board permits a phantom PROM operation to support bootstrap or diagnostic programs. MEMEX is supported to permit bank switching schemes. Finally, I/O port FF hexadecimal is decoded and gated onto the STD-Z80 Bus as MCSYNC*. This allows multiplex addressing for Z80 systems providing memory expansion beyond 64K of memory. This scheme is compatible with the COLEX STD-256DRAM and STD-128DRAM cards. Address, data and control buses are bidirectional to allow external DMA access to on-card memory.

COLEX AMERICA, INC. P.O. Box 801462, Dallas, Texas 75380, United States 214/458-2779
COLEX U.K., LTD. Index House, Ascot Berks, SL57EU, England, (0990)-23377
COLEX ASIA PACIFIC Luk Hop Industrial Bldg., 15th Floor, 8 Luk Hop St., San Po Kong, Kowloon, Hong Kong 3/7265651

STD-CPUE BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL

- Processor: Z80
- System Bus: STD-Z80
- System clock: 4.0 MHz
- Data bus: 8 bits, bi-directional
- Address bus: 16 bits standard with 8 bits extended (for multiplex bank select)
- Signal Loading: Inputs: One 74LS maximum
  Outputs: −3mA min @ 2.4 volts
  24mA min @ 0.5 volts
- Operating Temperature: 0°C to 60°C
- System Interrupt Units: 0 SIU's
- EPROM Timing Requirements: 249 ns from Output Enable
- I/O Address: Port FF hexadecimal used
- Power Requirements: @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	—	4.75	5.0	5.25	Volts
I_{CC}	@ 5V	—	487	725	mA*

*With no ROM/PROM/RAM installed in the sockets.

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- PC Board Thickness: 0.062 inch
- Connectors:
  STD-Bus (J1) — 56 pin card edge dual readout, 0.125 inch centers

ORDERING INFORMATION

Part Number	Description
STD-CPUE	4 MHz Z80 processor with 6 memory sockets
STM-CPUE	STD-CPUE Technical Manual

COLEX

CPUE

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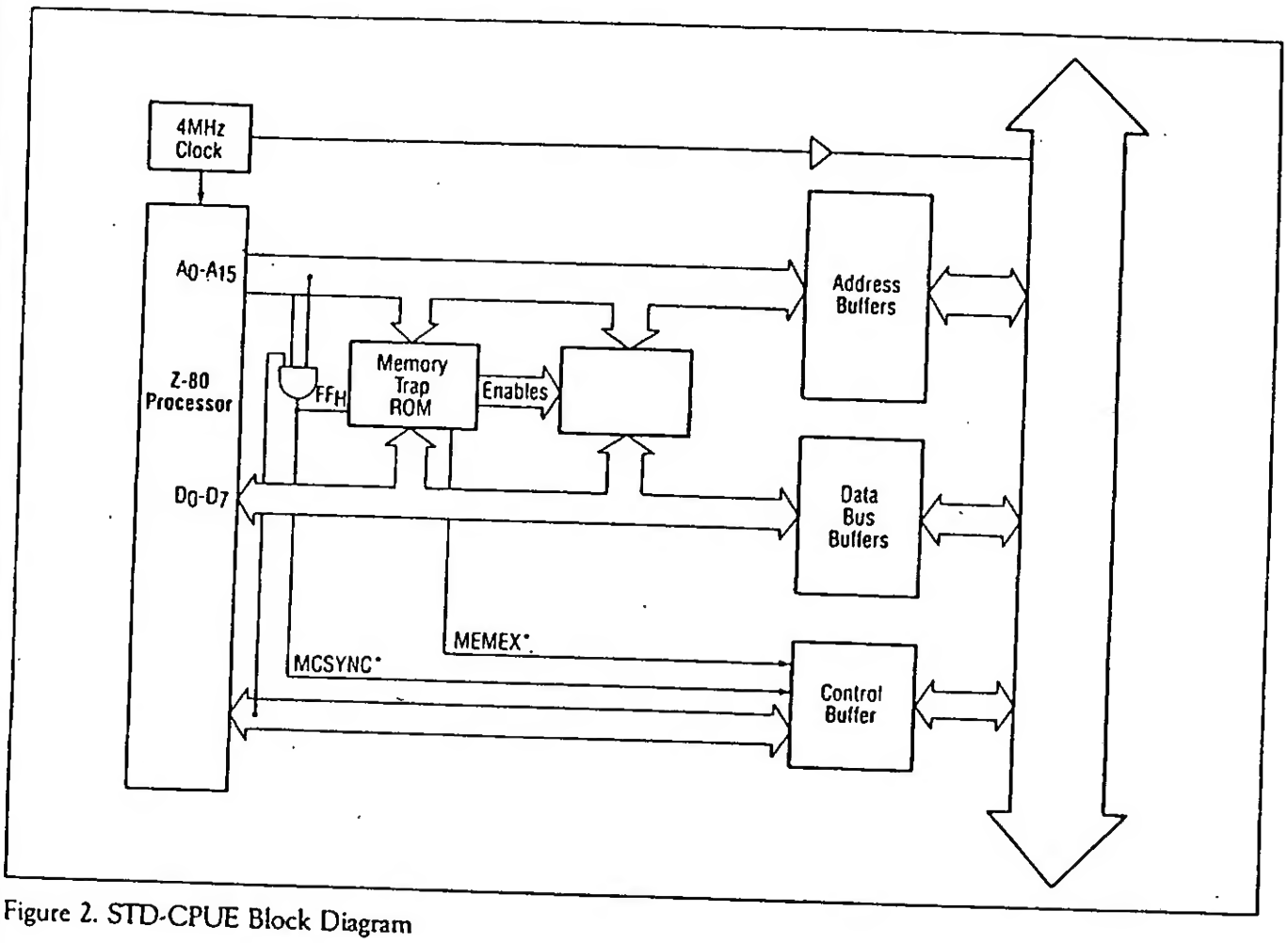


Figure 2. STD-CPUE Block Diagram

MEMORY SOCKET CONFIGURATION

The six memory sockets have six associated headers. These headers select the memory configuration on a socket by socket basis. These sockets accept the JEDEC 28-pin compatible ROMs, PROMs and RAMs. The configuration headers J2 through J7 pin outs are shown in Figure 3.

UX-22	11	12		/MEMRD
/OBM	9	10		/MEMWR
A11	7	8		UX-23
A14	5	6		VCC+5
UX-1	3	4		VCC+5
A13	1	2		UX-26

Figure 3. Memory Configuration Header (J2 through J7)

MEMORY SOCKET STRAPPING

Below are the strapping configurations for various device types. JX is the header corresponding from J2 through J7. Each socket must be strapped for the required device type.

Device Types	Straps Required
2716	JX - (2-4) (6-8) (11-12)
INTEL 2732	JX - (2-4) (7-8) (11-12)
INTEL 2764	JX - (3-4) (7-8) (11-12)
MX34000	JX - (2-4) (9-11)
MX37000	JX - (7-8) (9-11)
MK38000	JX - (1-2) (3-5) (7-8) (9-11)
NMC2116N-20	JX - (2-4) (8-10) (9-11)
2K x 8 RAM	JX - (2-4) (8-10) (11-12)
8K x 8 RAM	JX - (2-9) (7-8) (11-12)

Figure 4. Memory Strapping Chart

Both 24- and 28-pin devices can be placed in the sockets. The 24-pin devices are oriented toward the bottom of the socket as shown in Figure 5.

	28 PIN			
1	X		XX	28
2	X		XX	27
3	1	24-PIN	24	26
4	2		23	25
5	3		22	24
6	4		21	23
7	5		20	22
8	6		19	21
9	7		18	20
10	8		17	19
11	9		16	18
12	10		15	17
13	11		14	16
14	12		13	15

Figure 5. Memory Socket Reference

Each header is directly associated with a memory socket. The socket and header identification is below.

Socket	Header
U1	J2
U2	J3
U4	J4
U5	J5
U6	J6
U8	J7

Figure 6. Memory Sockets and Header Reference

STRAPPING OPTIONS

Figure 7 shows the locations of the memory sockets and associated headers.

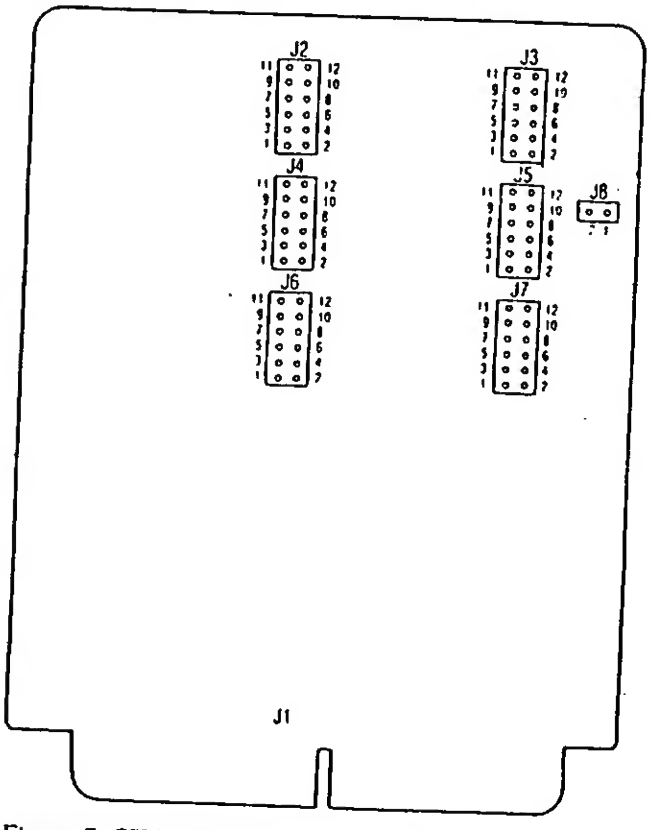


Figure 7. STD-CPUE Header Locations

MEMORY REFRESH

The STD-CPUE generates all address and control signals necessary to refresh STD Bus dynamic RAM cards. The REFRESH* occurs automatically during each OP code fetch and is transparent to system throughput and to cards not decoding the Refresh commands.

MEMORY MAP

The STD-CPUE card has a flexible memory map allowing it to support various on-board and off-board configurations. The Z80 has a standard direct addressing range of 64K bytes. The STD-CPUE can select 1 of 8 possible 64K byte configuration maps as shown in Figure 8. The smallest resolution in the map is 2K blocks. This map determines how each one of the six on-board memory sockets are to be addressed, as well as any additional off-board memory. The off-board memory is enabled by assertion of MEMEX*. This signal is decoded by other STD Bus memory cards and determines if the card can respond to the address. The on-board memory installed can be either ROM, PROM or RAM. The numbers in the brackets indicate the on-board sockets. Upon PBRESET* or at power up, Map 0 is always selected.

For example, Map 0 selects socket U1 for the first 8K memory addresses and then 5 additional sockets on 8K boundaries for memory addresses through $BFFF_H$. For memory addresses from $E800_H$ through $FFFF_H$, memory external to this board is addressable. This is used typically as a base page or common memory. Assertion of external memory is via the MEMEX* command which is indicated by the symbol ":M." During on-board memory cycles no MEMRQ* will be asserted on the STD Bus preventing dual address conflicts with other memory cards in a system.

Starting Memory Address	Map							
	0	1	2	3	4	5	6	7
F800	:M	[8]	:M	:M	:M	:M	:M	:M
F000	:M	[7]	:M	:M	:M	:M	:M	:M
E800	:M	[5]	:M	:M	:M	:M	:M	:M
E000		[4]	:M	:M				
D800			:M	:M				
D000			:M	:M				
C800			:M	:M				
C000			:M	:M				
B800	[8]		:M	:M				
B000	[8]		:M	:M				
A800	[8]		:M	:M				
A000	[8]		:M	:M				
9800	[7]		:M	:M				
9000	[7]		:M	:M				
8800	[7]		:M	:M				
8000	[7]		:M	:M				
7800	[5]		:M	:M				
7000	[5]		:M	:M				
6800	[5]		:M	:M				
6000	[5]		:M	:M				
5800	[4]		:M	:M				
5000	[4]		:M	:M				
4800	[4]		:M	:M				
4000	[4]		:M	:M				
3800	[2]	[2]	:M	[2]				
3000	[2]	[2]	:M	[2]				
2800	[2]	[2]	:M	[2]				
2000	[2]	[2]	:M	[2]				
1800	[1]	[1]	[1]	[1]				
1000	[1]	[1]	[1]	[1]				
0800	[1]	[1]	[1]	[1]				
0000	[1]	[1]	[1]	[1]				

Figure 8. STD-CPUE Memory Map Configuration

[ ] = STD-CPUE socket number
:M = MEMEX low (active) in this address space

Additional Memory configurations (Map 1 through Map 7) are possible by setting one mutually exclusive bit in Port FF_H. Figure 8 details the relation between the output bit and map selected.

Select Byte (Port FF_H)	Bank Selected (Off Board Memory)	Memory Map Selected	
		J8 Installed	J8 Removed
01	0	5	0
02	1	6	1
04	2	4	2
08	3	4	3
10	4	4	4
20	5	4	5
40	6	4	6
80	7	4	7

Figure 8. Memory Bank Select

Note: Only the above port selection bytes are permitted in port FF_H. Any other combination will cause dual addressing conflicts.

BANK SWITCHING

The Z80 has its memory capability extended beyond 64K bytes through a bank switching technique. Bank switching allows multiple pages of memory up to 64K bytes to reside in a system. These banks are enabled individually by setting a specific bit in I/O port FF_H. STD Bus systems can support up to 512K bytes of memory in eight 64K byte pages.

The STD-CPUE supports bank switching via Port FF_H. This same port serves a dual function for both bank switching and memory map configuration. COLEX has carefully selected the map configuration to allow maximum utilization with and without bank switching. Figure 8 shows the relation between the Port Select Byte, Bank Select and Memory Configuration Map.

J8 is defined as the Memory Map expansion jumper. When inserted, only three maps are available until a PBRESET* or power on occurs, which resets to Map 0. Removal of the jumper permits selection of all 8 memory configuration maps.

MEMORY MAP PROGRAMMING

If a special memory map is required for your application, refer either to the COLEX Application note or contact your local sales office for information on customized configuration of the memory map on the STD-CPUE.

MCSYNC*

The Colex STD-CPUE generates a signal called MCSYNC*. This signal is asserted whenever I/O Port FF_H is addressed. It is used to latch the data written to the port on memory cards such as the STD-128DRAM and STD-256DRAM for bank switching applications.

	Pin Numbers		
+5 V	2	1	+5 V
Ground	4	3	Ground
N.C.	6	5	N.C.
D7	8	7	D3
D6	10	9	D2
D5	12	11	D1
D4	14	13	D0
A15	16	15	A7
A14	18	17	A6
A13	20	19	A5
A12	22	21	A4
A11	24	23	A3
A10	26	25	A2
A9	28	27	A1
A8	30	29	A0
RD*	32	31	WR*
MEMRQ*	34	33	IORQ*
MEMEX	36	35	N.C.
MCSYNC*	38	37	REFRESH*
STATUS 0*	40	39	STATUS 1*
BUSRQ*	42	41	BUSAK*
INTRQ*	44	43	INTAK*
NMIRQ*	46	45	WAITRQ*
PBRESET*	48	47	SYSRESET*
CNTRL*	50	49	CLOCK*
PCI	52	51	PCO
N.C.	54	53	N.C.
N.C.	56	55	N.C.

Figure 9. STD-Z80 Bus Connector

SPECIFICATIONS

ELECTRICAL

- ☐ Processor: Z80
- ☐ System Bus: STD-Z80
- ☐ System Clock: 4.0 MHz
- ☐ Data Bus: 8 bits, bi-directional
- ☐ Address Bus: 16 bits standard with 8 bits extended (for multiplex bank select)
- ☐ Signal Loading: Inputs: One 74LS maximum
  Outputs: I_{OH}= 3mA min @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
- ☐ Operating Temperature: 0°C to 60°C
- ☐ System Interrupt Units: 0 SIU's
- ☐ EPROM Timing Requirements: 205ns from Output Enable
  375ns from Chip Enable
- ☐ I/O Address: Port FF hexadecimal used
- ☐ Power Requirements: @ 25°C

Parameter	Condition	Min.	Typ.	Max	Units
V_{cc}	-	4.75	5.0	5.25	Volts
I_{cc}	@ 5V	-	487	725	mA*

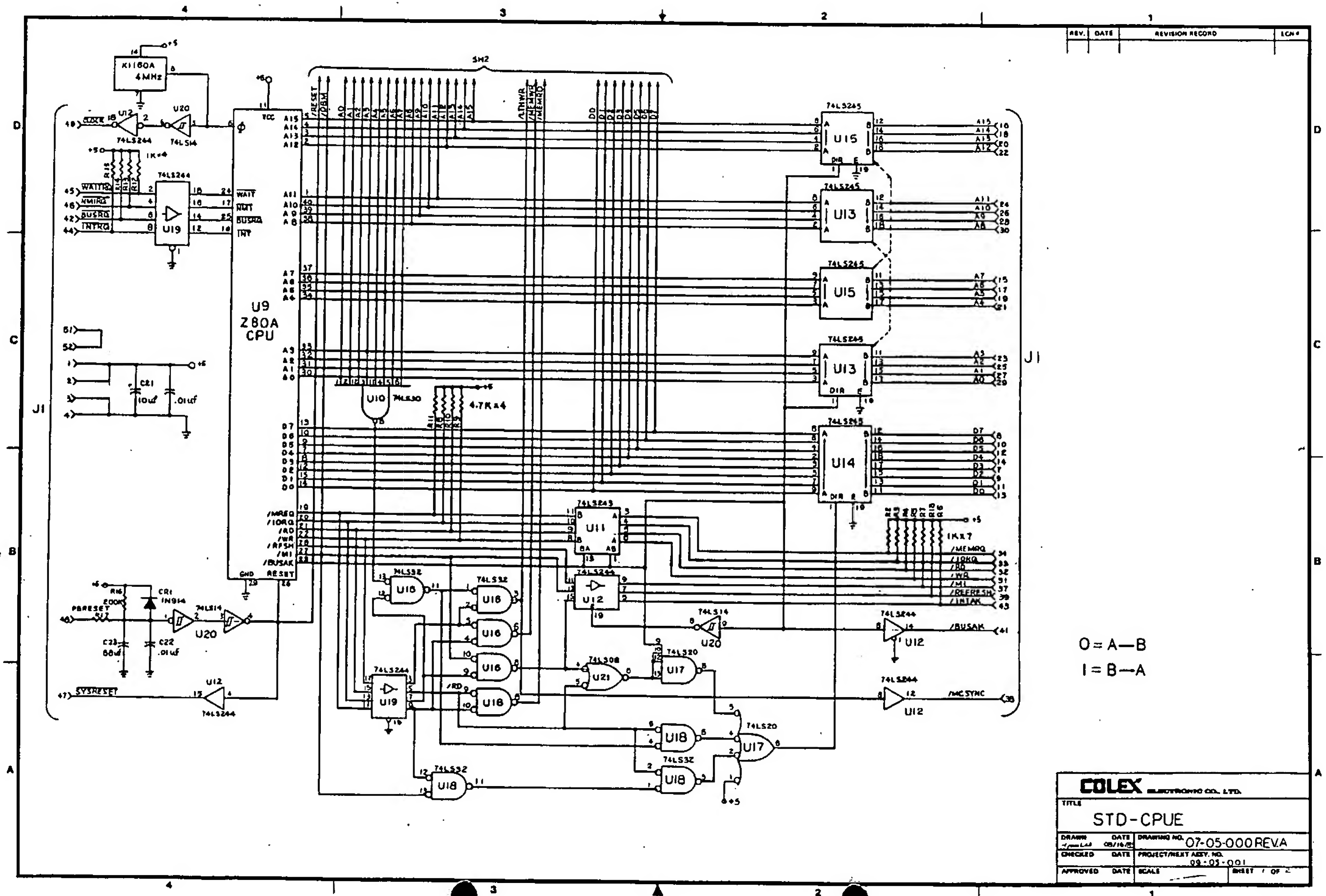
*With no ROM/PROM/RAM installed in the sockets.

MECHANICAL

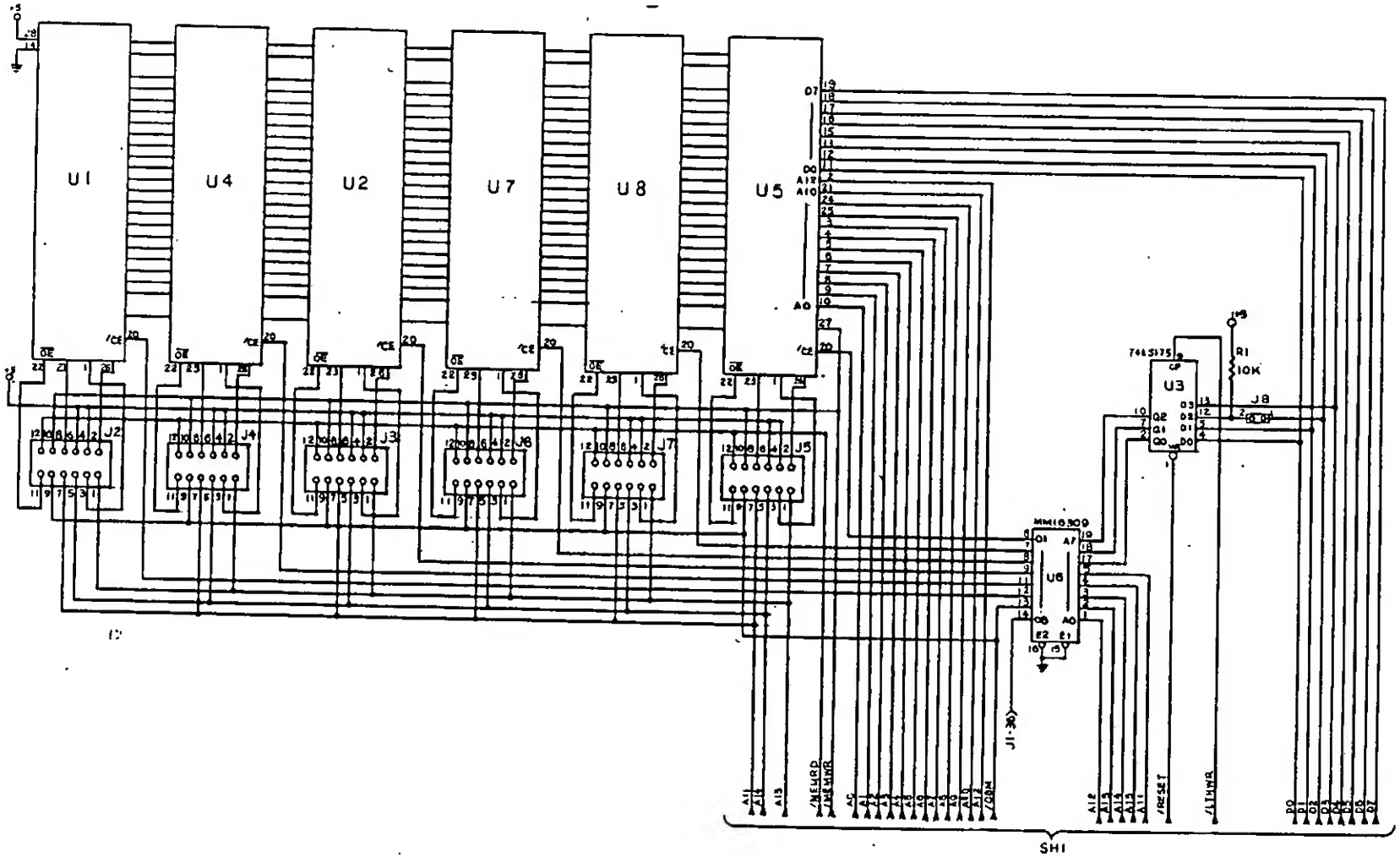
- ☐ Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ PC Board thickness: 0.062 inches
- ☐ Connectors:
  STD-Bus (J1): 56-pin card edge dual readout 0.125 inch centers



U9
Z80A
CPU
K1160A
4MHz
74LS244
74LS14
74LS245
74LS30
74LS32
74LS20
74LS30B
74LS243
4.7K x4
1K x4
1K x7
SH2
J1
/BUSAK
/MCSYNC
SYSRESET
PBRESET
0 = A—B
1 = B—A
COLEX ELECTRONIC CO. LTD.
TITLE
STD-CPUE
DRAWING NO. 07-05-000 REV.A
PROJECT/NEXT ASSY. NO. 09-05-001
REV. DATE REVISION RECORD



REV.	DATE	REVISION RECORD	ECN #

COLEX ELECTRONICS CO., LTD.

TITLE: STD-CPUE

DRAWN / DATE	09/16/87	DRAWING NO. 07-05-000REV.A
CHECKED / DATE		PROJECT/NEXT ASSY. NO. 09-05-001
APPROVED / DATE		SCALE / SHEET 1 OF 1